

AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application.

1. (Currently Amended) A half-rate clock and data recovery (CDR) circuit including:
 - a half-rate phase detector for detecting phases of an input signal and a half-rate clock;
and producing a comparison signal;
 - a charge pump circuit receiving the comparison signal and, in response, producing a pump signal;
 - a low-pass filter; receiving and filtering the pump signal to produce a control signal; and
 - a voltage controlled oscillator ~~for receiving the control signal and, in response,~~
generating the half-rate clock and feeding the half-rate clock back to the half-rate phase detector,
the half-rate phase detector comprising:
 - a first-stage latch circuit receiving the input signal and a second-stage latch
~~circuits; circuit receiving an output of the first-stage latch circuit,~~
 - an additional first-stage latch circuit receiving the input signal and an
additional second-stage latch circuit; circuit receiving an output of the additional first-stage
latch circuit,
 - a selector circuit which receives an output of the first-stage latch circuit and an
output of the additional first-stage latch circuit and outputs, in response, a re-timed signal ~~in~~
~~response;~~ synchronous with the half-rate clock and identical in array to the input signal,
 - a first exclusive OR circuit which receives an output of the second-stage latch
circuit and an output of the additional second-stage latch circuit and outputs a reference signal in
response;
 - a latch delay circuit in a through-data path; and receiving the input signal,
 - a one-pulse delay circuit in the through-data path, ~~and~~ receiving an output of the
latch delay circuit, ~~and outputting through-data for~~ generating a delay of one half-rate clock
pulse; and outputting through-data, thereby converting phase comparison polarity in the half-
rate phase detector, and
 - a second exclusive OR circuit which receives the re-timed signal from the
selector circuit and the through-data from the one-pulse delay circuit and outputs, in
response, an output signal ~~in response,~~ wherein the voltage controlled oscillator is an N type

LC voltage controlled oscillator ~~because of~~ for operation with the phase comparison polarity of the half-rate phase detector including inversion produced by the one-pulse delay circuit.

2. (Previously Presented) The half-rate CDR circuit according to Claim 1, wherein gate size of the one-pulse delay circuit of the half-rate phase detector is variable for adjustment of the delay of one pulse in the one-pulse delay circuit.

3. (Previously Presented) The half-rate CDR circuit according to Claim 1, wherein wiring length of the one-pulse delay circuit of the half-rate phase detector is variable for adjustment of the delay of one pulse in the one-pulse delay circuit.

4. (Previously Presented) The half-rate CDR circuit according to Claim 1, including a plurality of pump-up bias circuits having different gate bias levels, respectively, for a pump-up constant current source of the charge pump circuit and for changing current quantity of the pump-up constant current source upon switching of the pump-up bias circuits, for adjustment of the delay of one pulse in the one-pulse delay circuit.

5. (Previously Presented) The half-rate CDR circuit according to Claim 1, including a plurality of pump-down bias circuits having different gate bias levels, respectively, for a pump-down constant current source of the charge pump circuit and for changing current quantity of the pump-down constant current source upon switching of the pump-up bias circuits, for adjustment of the delay of one pulse in the one-pulse delay circuit.

6. (Previously Presented) The half-rate CDR circuit according to Claim 4, wherein the number of pump-up constant current sources of the charge pump circuit is changed to change the current quantity of the pump-up constant current sources for adjustment of the delay of one pulse in the one-pulse delay circuit.

7. (Previously Presented) The half-rate CDR circuit according to Claim 5, wherein the number of pump-down constant current sources of the charge pump circuit is changed to change the current quantity of the pump-down constant current sources for adjustment of the delay of one pulse in the one-pulse delay circuit.